CLAIMS

What is claimed is:

1. A Semiconductor device comprising:
- a semiconductor substrate having a top and a bottom surface,
- first and second insulating layer deposited on the top surface of said substrate,
- a runner arranged on top of the second insulator layer,
- a backside metal layer deposited on the bottom surface of the substrate,
- a first via structure extending from the bottom surface of the substrate to the top of the first insulating layer between the backside layer and the runner, and
- a second via structure extending from the top of the first insulating layer to the top of the second insulating layer between the first via and the runner.

2. The Semiconductor device as claimed in Claim 1, further comprising barrier metal layers arranged between the first and second via, between the runner and the second via, and between the first via and the backside metal layer.

3. The Semiconductor device as claimed in Claim 1, wherein the second via has a smaller footprint than the first via and a plurality of second vias are arranged between the first via and the runner.

4. The Semiconductor device as claimed in Claim 2, wherein said barrier metal layer between the first and second via has a cross-sectional profile of a saucer.

5. The Semiconductor device as claimed in Claim 4, wherein the bottom barrier metal layer comprises side walls that enclose said via.

6. The Semiconductor device as claimed in Claim 4, wherein the barrier metal layer between the first via and the second via comprises side walls that are spaced apart from said via.

7. The Semiconductor device as claimed in Claim 2, wherein the barrier metal layer between the first via and the second via consists of Titanium-Titanium nitride.

8. The Semiconductor device as claimed in Claim 2, wherein the barrier metal layer between the runner and the second via and the barrier metal layer between the backside layer and the first via consist of Titanium-Platinum.

9. The Semiconductor device as claimed in Claim 1, wherein the second via is filled with tungsten.

10. The Semiconductor device as claimed in Claim 13, wherein the first via is filled with Tungsten or copper.

11. The Semiconductor device as claimed in Claim 1, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

12. The Semiconductor device as claimed in Claim 1, wherein first and second via structures are arranged between a first and second stage of an integrated device for electromagnetic and /or thermal de-coupling.

13. The Semiconductor device as claimed in Claim 12, wherein the first stage is an input transistor stage and the second stage is a power transistor output stage.

14. The Semiconductor device as claimed in Claim 3, wherein the first via structure is extended in such a way that it at least partly surround a first device formed within said semiconductor device for electromagnetic and /or thermal de-coupling.

15. The Semiconductor device as claimed in Claim 14, wherein the first via structure is extended in such a way that it at completely surrounds said first device.

16. The Semiconductor device as claimed in Claim 14, wherein the first and second via structures are extended to form a grid including cells in which certain semiconductor devices are formed.

17. The Semiconductor device as claimed in Claim 14, wherein said first device includes an active semiconductor structure.

18. The Semiconductor device as claimed in Claim 14, wherein said first device includes a passive semiconductor structure.

19. The Semiconductor device as claimed in Claim 14, wherein the first device is shielded from a second device and the first device is coupled with the second device through at least one electrical coupling.

20. The Semiconductor device as claimed in Claim 19, wherein the second via structure comprises an opening for providing a passageway for the electrical coupling.

21. The Semiconductor device as claimed in Claim 19, wherein the electrical coupling is arranged in a first or second metal layer.

22. The Semiconductor device as claimed in Claim 1, wherein the first and second via structures are arranged within a field effect transistor structure having a source region, a drain region and a gate, in such a way that the first via couples the source region with the backside layer.

23. The Semiconductor device as claimed in Claim 22, further comprising at least one drain runner arranged on top of the first and/or second oxide layer above said drain region and on one side of the first and second via structures, and at least one gate runner arranged on top of the first and/or second oxide layer on the other side of the first and second via structures.

24. A Semiconductor device comprising:

- a semiconductor substrate having a top and a bottom surface,
- first and second insulating layer deposited on the top surface of said substrate,
- a first runner arranged on top of the first insulator layer,
- a second runner arranged on top of the second insulator layer above said first runner,
- a backside metal layer deposited on the bottom surface of the substrate,
- a first via structure extending from the bottom surface of the substrate to the top surface of the substrate between the backside layer and the first runner,
- a second via structure extending from the top surface of the substrate to the top of the first insulating layer between the first via and the first runner, and
- a third via structure extending from the top of the first insulating layer to the top of the second insulating layer between the first runner and the second runner.

25. The Semiconductor device as claimed in Claim 24, further comprising barrier metal layers arranged between the first and second via, between the first runner and the second via, between the first runner and the third via, between the third via and the second runner and between the first via and the backside metal layer.

26. The Semiconductor device as claimed in Claim 24, wherein the second and third vias have a smaller footprint than the first via and a plurality of second and third vias are arranged between the first via and the runner.

27. The Semiconductor device as claimed in Claim 25, wherein said barrier metal layer between the first and second via has a cross-sectional profile of a saucer.

28. The Semiconductor device as claimed in Claim 27, wherein the bottom barrier metal layer comprises side walls that enclose said via.

29. The Semiconductor device as claimed in Claim 27, wherein the barrier metal layer between the first via and the second via comprises side walls that are spaced apart from said via.

30. The Semiconductor device as claimed in Claim 25, wherein the barrier metal layers between the first via and the second via, between the first runner and the second via, and between the third via and the first runner consist of Titanium-Titanium nitride.

31. The Semiconductor device as claimed in Claim 25, wherein the barrier metal layers between the second runner and the third via and between the backside layer and the first via consist of Titanium-Platinum.

32. The Semiconductor device as claimed in Claim 24, wherein the second and third vias are filled with tungsten.

33. The Semiconductor device as claimed in Claim 24, wherein the first via is filled with Tungsten or copper.

34. The Semiconductor device as claimed in Claim 24, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

35. The Semiconductor device as claimed in Claim 24, wherein first, second and third via structures are arranged between a first and second stage of an integrated device for electromagnetic and /or thermal de-coupling.

36. The Semiconductor device as claimed in Claim 35, wherein the first stage is an input transistor stage and the second stage is a power transistor output stage.

37. The Semiconductor device as claimed in Claim 26, wherein the first via structure is extended in such a way that it at least partly surrounds a device formed within said semiconductor device for electromagnetic and /or thermal de-coupling.

38. The Semiconductor device as claimed in Claim 37, wherein the first via structure is extended in such a way that it at completely surround said device.

39. The Semiconductor device as claimed in Claim 37, wherein the first, second and third via structures are extended to form a grid including cells in which certain semiconductor devices are formed.

40. The Semiconductor device as claimed in Claim 37, wherein said device includes an active semiconductor structure.

41. The Semiconductor device as claimed in Claim 37, wherein said device includes a passive semiconductor structure.

42. The Semiconductor device as claimed in Claim 37, wherein the first device is shielded from a second device and the first device is coupled with the second device through at least one electrical coupling.

43. The Semiconductor device as claimed in Claim 42, wherein the second and/or third via structures comprise an opening for providing a passageway for the electrical coupling.

44. The Semiconductor device as claimed in Claim 43, wherein the electrical coupling is arranged in a first or second metal layer.

45. The Semiconductor device as claimed in Claim 24, wherein the first, second and third via structures are arranged within a field effect transistor structure having a source region, a drain region and a gate, in such a way that the first via couples the source region with the backside layer.

46. The Semiconductor device as claimed in Claim 45, further comprising at least one drain runner arranged on top of the first and/or second oxide layer above said drain region and on one side of the first and second via structures, and at least one gate runner arranged on top of the first and/or second oxide layer on the other side of the first, second and third via structures.

47. A method for manufacturing a semiconductor device comprising the steps of:

- providing a substrate,
- depositing an first insulating layer on top of said substrate,
- forming at least one window structure on top of said insulating layer,
- etching a first via within said substrate and through said insulating layer,
- filling said via with a metal,
- depositing a second insulating layer on top of said substrate,
- etching a second via within said second insulating layer on top of said first via,
- filling said second via with metal,
- planarizing the surface, and
- depositing a runner structure on top of said vias on said surface.

48. The method as claimed in Claim 47, further comprising the step of depositing a first barrier metal layer between said first via and said second via.

49. The method as claimed in Claim 47, further comprising the step of depositing a second barrier metal layer between said second via and said runner.

50. The method as claimed in Claim 48, wherein said first barrier metal layer has the cross-sectional profile of a saucer by overlapping the edges of said window.

51. The method as claimed in Claim 49, wherein the second barrier metal layer consists of Titanium-Platinum.

52. The method as claimed in Claim 48, wherein the first barrier metal layer consists of Titanium-Titanium nitride.

53. The method as claimed in Claim 47, wherein the first via is filled with copper or tungsten.

54. The method as claimed in Claim 47, wherein the second via is filled with tungsten.

55. The method as claimed in Claim 47, further comprising the steps of :

- grinding the bottom surface of said substrate to expose the metal within said via,
- depositing a backside metal layer on the bottom surface of said substrate.

56. The method as claimed in Claim 55, wherein the step of depositing the backside metal layer includes the steps of first depositing a metal barrier layer and then depositing a metal layer on top of the metal barrier layer.

57. A method for manufacturing a semiconductor device comprising the steps of:

- providing a substrate,
- forming at least one window structure on top of said substrate,
- etching a first via within said substrate,
- filling said via with a metal,
- depositing an first insulating layer on top of said substrate,
- forming at least one window structure on top of said first insulating layer,
- etching a second via through said insulating layer,
- filling said second via with a metal,
- depositing a first runner structure on top of said second via,
- depositing a second insulating layer on top of said substrate,
- forming at least one window structure on top of said second insulating layer,
- etching a third via within said second insulating layer on top of said second via,
- filling said third via with metal,
- planarizing the surface, and
- depositing a second runner structure on top of said stacked vias on said surface.

58. The method as claimed in Claim 57, further comprising the step of depositing a first barrier metal layer between said first via and said second via.

59. The method as claimed in Claim 57, further comprising the step of depositing a second barrier metal layer between said second via and said first runner, a third barrier metal layer between said first runner and said third via, and a fourth barrier metal layer between said third via and said second runner.

60. The method as claimed in Claim 58, wherein said first barrier metal layer has the cross-sectional profile of a saucer by overlapping the edges of said window.

61. The method as claimed in Claim 59, wherein the first, second and third barrier metal layers consist of Titanium-Titanium nitride and the fourth barrier metal layer consists of Titanium-Platinum .

62. The method as claimed in Claim 57, wherein the first via is filled with copper or tungsten.

63. The method as claimed in Claim 57, wherein the second and third vias are filled with tungsten.

64. The method as claimed in Claim 57, further comprising the steps of :

- grinding the bottom surface of said substrate to expose the metal within said first via,
- depositing a backside metal layer on the bottom surface of said substrate.

65. The method as claimed in Claim 64, wherein the step of depositing the backside metal layer includes the steps of first depositing a metal barrier layer and then depositing a metal layer on top of the metal barrier layer.

66. The method as claimed in Claim 65, wherein the backside metal barrier layer consists of Titanium-Platinum.